Description

Method for fabricating a contact hole plane in a memory module

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The invention relates to a method for fabricating a contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor. In this case, the invention relates in particular to a dynamic random access memory (DRAM).

DRAMs are composed of a multiplicity of memory cells which are formed regularly in the form of a matrix on a semiconductor wafer. Said memory cells generally comprise a storage capacitor and a selection transistor. During a read or write operation, the storage capacitor is charged or discharged, via the selection transistor, with an electrical charge corresponding to the respective data unit (Bit). For this purpose, the selection transistor is addressed with the aid of a bit line and a word line.

DRAMs are generally realized with the aid of planar technology. The latter comprises a sequence of individual processes which in each case act over the whole area at the surface of the semiconductor wafer and, by means of suitable masking layers, lead in a targeted manner to the local alteration of the semiconductor material. In this case, the selection transistor of the memory cell is generally embodied as a field-effect transistor, with two highly doped diffusion regions in the semiconductor wafer, which form the source/drain electrodes. A channel is formed between these two diffusion regions, via which channel an electrically conductive connection can be produced with the aid of a gate electrode formed above the channel. In the case of DRAMs, the gate electrodes of the field-effect transistors are realized as gate

electrode tracks which run parallel and form the word
lines of the DRAM. The bit lines then run transversely
over said gate electrode tracks, a conductive connection
between a bit line and a source/drain electrode of the
5   selection transistor of a corresponding memory cell being
produced in the interspace between two gate electrode
tracks.

The bit line contact is usually fabricated as a so-called
10   "self-aligned" contact in the DRAM process. A possible
process sequence for forming such bit line contacts is
illustrated diagrammatically in Figure 4. Figures 4A to
4D respectively show a cross section through a silicon
wafer after various successive process steps for forming
15   the bit line contacts. The starting point is the
prepatterned silicon wafer 1, on which gate electrode
tracks 2 spaced apart equidistantly have been formed.
These gate tracks 2 generally comprise a conductive layer
stack 21 covered by a silicon nitride cap 22. Insulating
20   spacers 23, preferably made of silicon nitride, are
formed at the sidewalls of the gate electrode tracks 2. A
cross section through the correspondingly prepatterned
silicon wafer is shown in Figure 4A.

25   A further silicon nitride layer 300 is deposited in a
first step for forming the bit line contacts. In order to
define the region of the bit line contacts on the silicon
wafer 1, a mask layer sequence 350, 400 is subsequently
produced, and completely covers the bit line contacts.
30   Figure 4B shows a cross section through the silicon wafer
1 after this process step.

With the aid of a lithography step, the regions at which
the bit line contacts of the selection transistors are
35   later intended to be produced are then defined on the

mask layer sequence 350, 400. These regions of the mask
layer sequence 350, 400 are then opened with the aid of a
selective etching. By means of a further etching, the
silicon nitride layer 300 is then removed in the opening
5   regions of the mask layer sequence 350, 400. The
resultant silicon wafer configuration is shown in Figure
4C. During the silicon nitride etching, the silicon
nitride layer 300 is etched away essentially only at the
horizontal areas, but remains at the sidewalls of the
10   gate electrode tracks 2, as is shown in Figure 4C.

In a final process step, the contact openings are then
filled with a conductive material in order to fabricate
the bit line contacts 9. A cross section through the
15   silicon wafer 1 after the production of the bit line
contacts 9 is shown in Figure 4D.

Such a standard process for producing bit line contacts
is known inter alia from WO 01/09946. This standard
20   process essentially has three significant disadvantages.
The distance between two mutually adjacent gate electrode
tracks between which the bit line contact is intended to
be embodied is additionally decreased by the silicon
nitride spacers at the sidewalls of the gate electrode
25   tracks. This gap narrowing increases the aspect ratio,
that is to say the ratio of width to height of the
contact openings, as a result of which processes that are
to be performed in the contact openings become
increasingly more difficult. This problem is intensified
30   from DRAM generation to DRAM generation on account of the
ever smaller lateral dimensions. Furthermore, owing to
its high dielectric constant, the silicon nitride spacer
in the contact hole leads to a strong coupling between
the conductive material in the bit line contact and the
35   gate electrode tracks, so that there is the risk of the

electrical properties of the memory cells being impaired.
The use of silicon nitride as a spacer for forming the
bit line contacts has the disadvantage, moreover, that,
on account of the directional etching required, an
5. etching process with a high sputtering element is
required, it being possible for the gate electrode tracks
to be attacked and damaged particularly in the upper edge
region.

10 Therefore, it is an objective of the invention to provide
an optimised process implementation for fabricating bit
line contacts in a memory module, said process
implementation being distinguished by a low coupling
capacitance between bit line contacts and gate electrode
15 tracks and furthermore enabling a reliable and
damage-free bit line contact fabrication in a simple
manner.

A method having the features of the preamble of claims 1,
20 19, 22 and 25 is known from US 6 287 905 B2. Further
methods for fabricating a contact hole plane are known
from   US 2003/0008453 A1,   DE 102 23 748 A1,
DE 199 35 852 A1, US 6 171 954 B1 and US 6 096 633.

25 This object is achieved by means of a method in
accordance with claim 1, 19, 22 or 25. Preferred
developments are specified in the dependent claims.

According to the invention, in order to fabricate a
30 contact hole plane in a memory module with an arrangement
of memory cells each having a selection transistor, the
following method steps are performed:
provision of a semiconductor substrate with an
arrangement of mutually adjacent gate electrode tracks on
35 the semiconductor surface;

production of an insulator layer on the semiconductor
surface;

formation of a sacrificial layer on the insulator layer,
the regions between the mutually adjacent gate electrode
5   tracks essentially being filled and the gate electrode
tracks being covered;

formation of material plugs on the sacrificial layer for
the purpose of defining contact openings between the
mutually adjacent gate electrode tracks;

10   anisotropic etching of the sacrificial layer, the
material plugs with the underlying sacrificial layer
blocks remaining;

production of a vitreous layer with uncovering of the
sacrificial layer blocks above the contact openings
15   between the mutually adjacent gate electrode tracks, the
regions between the mutually adjacent gate electrode
tracks essentially being filled and an essentially planar
surface being formed;

etching of sacrificial layer material from the vitreous
20   layer for the purpose of removing the sacrificial layer
blocks above the contact openings between the mutually
adjacent gate electrode tracks;

removal of the uncovered insulator layer above the
contact openings on the semiconductor surface between the
25   mutually adjacent gate electrode tracks; and

filling of the contact opening regions with a conductive
material, in the process forming an essentially planar
surface with the surrounding vitreous layer.

30   The process implementation according to the invention
makes it possible to completely dispense with the use of
a silicon nitride spacer for forming the bit line
contacts between the gate electrode tracks running
parallel. Instead, it is possible to use material
35   spacers, as specified in a preferred embodiment, for

example silicon dioxide spacers as insulating spacers
which are distinguished, by comparison with silicon
nitride spacers, by a significantly smaller dielectric
constant and thus a reduced coupling between the
5   conductive material in the bit line contacts and the gate
electrode tracks. The sacrificial layer etching - carried
out in the process implementation - for opening the
contact hole in the vitreous layer is distinguished by a
high selectivity during etching, it not being necessary
10 to carry out patterning with the aid of the etching
process and thus essentially no sputtering element being
necessary during the etching process. This ensures that
the gate electrode tracks are not damaged during the
contact hole opening.
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In accordance with a preferred embodiment, in order to
produce the vitreous layer with uncovering of the
sacrificial layer blocks above the contact openings
between the mutually adjacent gate electrode tracks, the
20 following method steps are carried out:
removal of the uncovered insulator layer on the
semiconductor surface between the mutually adjacent gate
electrode tracks;
production of dopings in predetermined regions of the
25 uncovered semiconductor surface between the mutually
adjacent gate electrode tracks for the purpose of forming
the selection transistors;
production of an existing liner layer;
formation of the vitreous layer on the liner layer, the
30 regions between the mutually adjacent gate electrode
tracks essentially being filled; and
planarization of the vitreous layer with uncovering of
the sacrificial layer blocks above the contact openings
between the mutually adjacent gate electrode tracks, the
35 essentially planar surface being formed.

This procedure represents a particularly effective and cost-effective process implementation in order to form, with the aid of the vitreous layer, a reliable etching
5   mask for the subsequent removal of the sacrificial layer blocks.

In accordance with one embodiment, the polysilicon layer is produced on the insulator layer in this case in the
10 following manner. A first sacrificial layer is deposited on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered. The first sacrificial layer is then planarized with uncovering of
15 the gate electrode tracks, an essentially planar surface being formed. Finally, a second sacrificial layer is deposited, the layer thickness of the second sacrificial layer preferably being 200 to 1000 nm.

20 This procedure provides for a homogenous and highly planar sacrificial layer surface which makes it possible to form even extremely small free-standing resist structures without the latter falling over on account of unevennesses of the underlying sacrificial layer. In
25 particular, this procedure makes it possible to reliably produce, below the resist layer, an ARC layer, which provides for improved resist adhesion and exposure, with a predetermined thickness and a high accuracy. Furthermore, the first sacrificial layer may be
30 planarized by using a chemical mechanical polishing method using a stop polishing technique, said method being stopped by the nitride covering layer of the gate electrode tracks. This chemical mechanical polishing provides for a high surface planarity.

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In accordance with an alternative embodiment, the
sacrificial layer is formed on the insulator layer by
means of the following method steps. Firstly, the
sacrificial layer is deposited on the insulator layer,
5   the regions between the mutually adjacent gate electrode
tracks being filled and the gate electrode tracks being
covered. The sacrificial layer is then planarized, the
gate electrode tracks with a layer thickness of
preferably 200 to 1000 nm remaining covered and an
10   essentially planar surface being formed.

This procedure once again makes it possible to form a
highly planar sacrificial layer surface for forming even
extremely small resist structures preferably with the aid
15   of a previously applied resist layer, the method
presented requiring only a single sacrificial layer
application and it being possible to use a cost-effective
so-called blind polishing process during the chemical
mechanical polishing, i.e. a planarization stop after a
20   predetermined time in the polysilicon layer.

In accordance with a further preferred embodiment, the
material plugs are formed on the sacrificial layer for
the purpose of defining the contact openings between the
25   mutually adjacent gate electrode tracks by means of the
following method steps. Firstly, preferably an ARC layer
is deposited on the sacrificial layer. A resist layer is
then applied on the ARC layer and is subsequently exposed
by means of a mask which defines the contact openings
30   between the mutually adjacent gate electrodes, and the
resist layer is then developed in order to remove the
exposed regions of the resist layer and to form the
material plugs made from resist material on the
polysilicon layer for the purpose of defining contact
35   openings between the mutually adjacent gate electrode

tracks. This procedure makes it possible to form material plugs in a precisely defined form for the purpose of defining the contact openings for the bit line contacts between the gate electrode tracks with the aid of a

5   photoresist layer.

In accordance with an alternative embodiment, it is possible to fabricate the material plugs on the sacrificial layer in the following manner. Firstly, a

10   hard mask layer is deposited on the sacrificial layer and then a resist layer is deposited on the hard mask layer. The resist layer is subsequently exposed by means of a mask which defines the contact openings between the mutually adjacent gate electrode tracks. The resist layer

15   is then developed in order to remove the exposed regions of the resist layer and to uncover the hard mask layer. The patterned resist layer is transferred into the hard mask layer by means of anisotropic etching. Afterward, the patterned resist layer is removed and a filling

20   material is introduced into the etching openings of the hard mask layer. After the removal of the hard mask layer, material plugs made from the filling material then remain on the sacrificial layer, which define the contact openings between the mutually adjacent gate electrode

25   tracks.

This inversive formation of the material plugs made from a filling material enables even extremely small plug structures to be fabricated reliably. The additionally

30   applied hard mask layer serves as a further sacrificial layer in which openings which are predefined by means of a lithography step are produced by etching. By filling these openings with a filling material and subsequently removing the hard mask layer, highly precise material

35   plug structures are formed. What is advantageous about

this procedure is that it is possible to dispense with
planarizing the sacrificial layer lying below the hard
mask layer. Furthermore, by means of the hard mask layer,
it is possible to set the plug height exactly to a

5   desired height which is optimal for the subsequent
process steps. What is more, a high etching resistance
during the hard mask etching can be achieved through a
suitable choice of the filling material.

10 In accordance with a preferred embodiment, a vitreous
layer is used as the hard mask layer. The use of such an
optically transparent hard mask layer in the case of a
nonplanar base of the sacrificial layer makes it possible
to utilize steps in the sacrificial layer for alignment

15 and overlay measurements of the contact hole lithography.

In accordance with a preferred embodiment, polysilicon is
preferably used as the material for the sacrificial
layer. Polysilicon enables a particularly high

20 selectivity when etching free the contact hole openings
in the vitreous layer, it being possible to carry out the
etching process with a very low sputtering element,
thereby preventing the contact hole opening from being
damaged during the etching process.

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In accordance with a further preferred embodiment, a
carbon-based layer is used as the sacrificial layer in
the contact openings. Carbon enables an oxide etching in
a standard dry etching chamber, as a result of which a

30 particularly high selectivity can be achieved. What is
more, carbon layers are distinguished by a particularly
favorable deposition behavior, a high planarity being
established. This provides for a cost-effective layer
application process. In this case, furthermore, a

35 dielectric layer is preferably to be additionally applied

on the carbon-based layer. This additional dielectric mask layer provides for a high selectivity both with respect to the overlying lithography mask and with respect to the underlying carbon layer and thus for an
5   improvement in the etching behavior.

The invention is explained in more detail with reference to the accompanying drawings, in which

Figures 1A to 1O show one possible embodiment of a
10   process sequence according to the invention for fabricating a contact hole plane in a memory module, diagrammatic cross sections through the silicon wafer in different process stages of the process sequence respectively being shown;

15   Figures 2A to 2G show an alternative embodiment of the process sequence according to the invention with regard to the formation of the material plugs on the polysilicon layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks, the
20   individual figures respectively showing a diagrammatic cross section through the silicon wafer after different process stages;

Figures 3A to 3D show a further embodiment of the process sequence according to the invention with regard to the
25   formation of the metal plugs, use being made of a carbon layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks and the individual figures respectively showing a diagrammatic cross section through the silicon wafer in
30   different process stages of the process sequence; and

Figures 4A to 4D show a conventional method for forming bit line contacts between gate electrode tracks of a memory module, the individual figures respectively showing cross sections through the. silicon wafer after
35   different process stages.

The invention is illustrated by way of example using a
process sequence for fabricating a contact hole plane in
a DRAM module with a memory cell region and a logic
region on a silicon wafer. However the invention can be
used to form any desired contacts between gate electrode
tracks in semiconductor modules.

Figures 1A to 1O respectively show a cross section
through a detail from a prepatterned silicon wafer 1, on
which a memory cell region and a peripheral logic region
are provided. In this case, the memory cells of the DRAM
are composed of a selection transistor and a storage
capacitor. The peripheral logic region contains various
components for driving the memory cells.

Figure 1A shows the starting point, the prepatterned
silicon wafer 1 (structures are not shown), on which are
formed a cell array, represented by four gate electrode
tracks 2 spaced apart equidistantly, and a logic region
separate therefrom, represented by a further gate
electrode track 20. In particular, the storage
capacitors, preferably formed as trench capacitors, have
already been provided in the region of the memory cell
array of the silicon wafer 1. The gate electrode tracks
2, which form the word lines in the cell array, are
generally composed of a layer stack, comprising a
conductive layer 21 and a covering layer 22. In this
case, the conductive layer 21 may comprise a metal or
else a doped polysilicon. The covering layer 22 is
preferably fabricated from silicon nitride.

In a first process step, a silicon dioxide layer 3 is
applied to said silicon wafer 1 with the gate electrode
tracks 2, 20 prepatterned in such a way. In this case,

the silicon dioxide layer 3 is preferably applied with
the aid of the so-called LPCVD method, which ensures a
high conformity of the silicon dioxide layer 3. The
silicon dioxide layer 3 serves as an insulating spacer
5   between the gate electrode tracks 2. A cross section
through the silicon wafer 1 after this process step is
shown in Figure 1B.

Afterward, a polysilicon layer 4 is deposited in
10 large-area fashion on the silicon dioxide layer 3 in a
further process step, likewise preferably with the aid of
the LPCVD method. In this case, the layer thickness of
the polysilicon layer 4 is preferably at least one to
three times the height of the gate electrode tracks 2. A
15 cross section through the silicon wafer after this
process step is illustrated in Figure 1C. In this case,
the surface of the polysilicon layer 4 exhibits a
residual topology of the structure of the underlying gate
electrode tracks 2 on the silicon wafer 1.
20

In a further process step, the surface of the polysilicon
layer 4 is then planarized in order to obtain a planar
surface. A chemical mechanical polishing process is
preferably used for this purpose, it being possible to
25 achieve a particularly high planarity by using a
so-called stop polishing process. In this case, the
chemical mechanical polishing operation is automatically
curbed to a great extent upon impinging on the underlying
layer and can thus be ended. A particularly advantageous
30 stop polishing process can be achieved by means of a stop
on the nitride covering layer 22 of the gate electrode
track 2. A particularly planar surface then results, as
is shown in Figure 1D, the silicon dioxide layer 3 having
been concomitantly polished down from the gate electrode

track 2, 20 and the nitride covering layer 22 of the gate
electrode tracks 2, 20 being uncovered.

Afterward, in a further deposition process, preferably
5   again with the aid of the LPCVD method, a further
polysilicon layer 5 with a layer thickness of 200 to
1000 nm, preferably 300 to 400 nm, is deposited on the
first polysilicon layer 4. This results in a highly
planar covering of the gate electrode track structure 2
10   on the silicon wafer 1. A cross section through the
silicon wafer 1 after this process step is illustrated in
Figure 1E.

As an alterative to the illustrated process sequence with
15   two polysilicon layers 4, 5 for forming a plane
polysilicon layer covering the gate electrode track
structure, it is also possible to perform only a single
polysilicon deposition and to provide, instead of a
chemical mechanical polishing operation according to the
20   stop polishing method, a blind polishing process of the
polysilicon layer 4, during which the chemical mechanical
polishing operation is stopped in the polysilicon layer 4
itself in a predetermined thickness above the gate
electrode tracks 2, 20. In this case, once again a
25   polysilicon thickness above the gate electrode tracks of
200 to 1000 nm, preferably 300 to 400 nm, is preferably
intended to remain. What is advantageous about this
alternative embodiment is that only a single polysilicon
deposition process has to be performed, but the planarity
30   is impaired by comparison with a polysilicon application
with two successive deposition processes.

In a further process sequence, the region of the bit line
contacts for the connection of the selection transistors
35   of the memory cells in the silicon wafer 1 is defined on

the plane polysilicon layer 5. This is preferably performed with the aid of lithography technology. In a first step, preferably an ARC layer 61 is applied and then a resist layer 62 is applied. The ARC layer 61

5   provides for an improved exposure of the resist layer 62 since the ARC layer 61 essentially prevents reflection of light at the interface. Furthermore, the ARC layer 61 ensures an improved adhesion of the resist material 62. The applied resist layer 61 is exposed with the aid of a

10 mask which defines the regions in which the contact openings between the mutually adjacent gate electrode tracks 2 are intended to be formed. Afterward, the resist layer 62 is developed, the exposed resist structures being stripped away. The result then is a cross section

15 through the silicon wafer 1 as is shown in Figure 1F, in which resist plugs 6 remain on the polysilicon layer 5 above the contact openings for the bit line contact between the mutually adjacent gate electrode tracks. This procedure makes it possible to produce even extremely

20 small resist plugs having a diameter of less than 150 nm without the resist plugs falling over on account of inadequate adhesion.

As an alternative to the use of resist plugs 6, it is

25 also possible to form hard mask blocks above the contact opening regions. In order to form the hard mask blocks, a hard mask layer is applied to the plane polysilicon layer 5 and is then patterned with the aid of a lithography process. For this purpose, a resist layer is applied,

30 which is exposed with the aid of a mask which defines the regions in which the contact openings between the mutually adjacent gate electrode tracks 2 are intended to be formed. Afterward, the resist layer is developed, the exposed resist structures being stripped away outside the

35 contact opening regions. Then, with the aid of a

selective etching, the hard mask layer is etched away at
the uncovered surface regions and the residual resist
layer is subsequently removed, so that material plugs
remain similarly to the resist plugs 6 in Figure 1F.

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Using the resist plugs 6 or the alternatively fabricated
hard mask plugs as a mask, an anisotropic polysilicon
etching is then carried out in a next process step,
during which the polysilicon layers 4, 5 are completely
10   removed outside the regions concealed by the resist plugs
6. This anisotropic polysilicon etching for producing
blocks 6 in the region of the envisaged contact openings
for the bit line contacts, comprising polysilicon blocks
with resist covering, is highly selective with respect to
15   silicon dioxide and silicon nitride, so that the silicon
dioxide layer 3 on the silicon wafer 1 and the uncovered
nitride covering layers 22 of the gate electrode tracks
2, 20 are not attacked. A cross section through the
silicon wafer 1 after the anisotropic polysilicon etching
20   is shown in Figure 1G.

Afterward, the remaining resist plug layer 61 is removed
by means of a resist etching. The uncovered silicon
dioxide layer 3 on the silicon wafer 1 is then removed
25   anisotropically, as a result of which the surface of the
silicon wafer 1 is uncovered. The silicon dioxide layer 3
in the region of the sidewalls of the gate electrode
tracks 2, 20 remains, however. A cross section through
the silicon wafer 1 after the process step explained last
30   is illustrated in Figure 1H.

Through the uncovered surfaces of the silicon wafer 1,
standard processes for forming DRAM components are then
used to perform the desired dopings in the silicon
35   surface, in particular also for the selection transistors

of the memory cells. After the formation of the doped
regions in the silicon surface, in a next process step, a
liner layer 7 is applied as a diffusion barrier,
preferably a silicon nitride layer. A vitreous layer,
5   preferably a BPSG layer 8, is then deposited on said
silicon nitride layer 7, and is subjected to a heating
step for the purpose of densification and planarization.
A cross section through the silicon wafer 1 after the
temperature reflow of the BPSG layer 8 is shown in Figure
10 1I.

Afterward, a planarization of the BPSG layer 8 is then
performed with the aid of a chemical mechanical polishing
operation. In this case, the chemical mechanical
15 polishing operation is preferably designed such that it
is stopped by means of an end point determination. In
this case, the end point determination used may be an
ammonia signal which arises if the silicon nitride liner
layer 7 on the polysilicon plugs 4, 5 is polished away
20 during the chemical mechanical polishing operation. A
cross section through the silicon wafer 1 after the
planarization of the BPSG layer is shown in Figure 1J.
The BPSG layer then forms a highly plane surface, the
surface of the polysilicon blocks 4, 5, which are
25 arranged above the contact openings for the bit line
contacts to the selection transistors of the memory
cells, being uncovered.

In a further process sequence, the surface of the silicon
30 wafer 1 is opened in the region of the contact openings
for the bit line contacts. For this purpose, in a first
step, by means of an etching, the polysilicon 4, 5 is
completely removed from the contact opening. This
polysilicon etching can be carried out highly selectively
35 since there is no need to perform a patterning of the

polysilicon layer, rather the only objective is to
completely remove the polysilicon. Therefore, there is
also no need for the polysilicon etching process to
contain any sputtering components. In this case, the
5   polysilicon etching is preferably carried out as a dry
etching. A cross section through the silicon wafer 1
after the removal of the polysilicon blocks from the
contact openings is illustrated in cross section in
Figure 1K.
10

Afterward, the silicon dioxide layer 3 at the bottom of
the uncovered contact openings is then removed with the
aid of a further etching step, as is shown in Figure 1L.
This process of etching free the silicon wafer surface is
15   preferably effected by using a highly selective silicon
dioxide etching process which is distinguished by a
particularly good etching behavior of silicon dioxide in
the region of deep contact openings. Such a silicon
dioxide etching process with a high etching rate in the
20   region of high aspect ratios ensures that, in particular,
the BPSG layer 8 is not attacked during etching. What is
more, the silicon dioxide spacers remain at the sidewalls
of the gate electrode tracks 2 in the region of the
contact openings. As an alternative to such a silicon
25   dioxide etching process with high selectivity in the
contact hole region, it is also possible to use a
standard silicon dioxide etching process, which then also
attacks the BPSG covering layer 8. The thickness of the
BPSG covering layer must then be designed such that it
30   suffices to enable a corresponding etching removal
without the underlying gate electrode tracks 2 being
uncovered.

Afterward, by means of a further process sequence known
35   from the standard DRAM fabrication process, contact is

made with the components in the logic region. The
contacts to the logic components in the peripheral region
of the DRAM are formed with the aid of conventional
contact hole lithography. A substrate contact 10 is shown
5   by way of example in Figure 1M. In addition, connections
are also produced to the gate electrode tracks 20 in the
logic region (not shown).

In order to form the contacts to the components in the
10   silicon wafer 1, all of the contact openings are then
filled with a conductive material, e.g. a metal such as
tungsten. All known metal deposition methods may be used
in this case. In the case of a tungsten filling, it is
possible, by way of example, firstly to use a tungsten
15   liner and then to perform a large-area filling, the metal
layer then being removed again as far as the surface of
the BPSG layer 8, thereby producing a cross section
through the silicon wafer 1 as is shown in Figure 1N, in
which the contact openings 9, 10 are filled with a
20   conductive metal block. Finally, a further large-area
deposition of a conductive material, in particular of a
metal such as tungsten or aluminum, is then performed in
a further process sequence for forming the first
metallization plane M0. This metal plane is then
25   patterned with the aid of photolithography in order to
form the wiring of the bit line contacts 9 in the first
wiring plane 11. Between the individual interconnects 10,
provision is preferably made of a silicon dioxide layer
12 for insulating the interconnects. A cross section
30   through the silicon wafer 1 after the last-mentioned step
is shown in Figure 10. Further metallization planes for
the wiring of the individual components are then
performed in the context of the design of the DRAM
process.

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The process sequence illustrated makes it possible, in
the case of producing bit line contacts in the cell array
of a DRAM, to achieve three significant advantages over
the conventional method, as is illustrated in cross
5   section using the example of a silicon wafer 1 in Figures
3A to 3D. A silicon dioxide spacer 3 is used instead of
the silicon nitride liner 300 as spacer between the gate
electrode tracks 2, as is used in the standard process
and is shown in Figure 4B. Said silicon dioxide spacer 3
10 is distinguished by a lower dielectric constant and thus
a reduced coupling between the conductive filling
material of the bit line contacts and the adjacent gate
electrode tracks by comparison with the silicon nitride
spacer 300. This reduced electrical coupling between the
15 bit line contacts and the gate electrode tracks ensures
that the electrical properties of the DRAM are not
impaired. This is a significant advantage in particular
with regard to the advancing miniaturization of the
lateral DRAM dimensions in the course of higher memory
20 cell integration.

What is more, the use of an individual silicon dioxide
layer 3 as spacer between the adjacent gate electrode
tracks 2 in the region of the bit line contact, by
25 comparison with the silicon nitride liner 300
conventionally used, largely avoids a limitation of the
contact hole width, which results in a higher aspect
ratio and thus in greater difficulties during the
processes to be performed in the contact openings. The
30 use of a polysilicon layer 4, 5 for forming polysilicon
blocks in the envisaged contact openings, which are then
removed again in order to fill the contact openings,
makes it possible to use highly selective etching
processes which, in particular, avoid damage to the gate
35 electrode tracks 2. The formation of polysilicon blocks

4, 5 enclosed by a BPSG layer 8 with a silicon nitride liner 7 makes it possible to use etching processes which etch polysilicon in an unpatterned manner. This makes it possible to avoid the use of sputtering components during

5   the etching process, which can lead to damage to the open regions of the gate electrode tracks 2.

Figures 2A to 2G illustrate an alternative embodiment for fabricating the polysilicon blocks in the contact opening

10   regions. This alternative procedure ensures a particularly reliable formation of the polysilicon plugs for protecting the contact openings.

In order to form the polysilicon blocks for protecting

15   the contact openings, the method commences in a process stage as is illustrated in Figure 1C in connection with the first embodiment. On the silicon wafer 1, the prepatterned gate electrode tracks 2, are provided with a silicon dioxide layer 3 and filled with a polysilicon

20   layer 40, the polysilicon layer 40 completely covering the gate electrode tracks 2 but exhibiting the topology of the gate electrode tracks at the surface in attenuated fashion. A cross section through the silicon wafer 1 after this process is illustrated in Figure 2A.

25
Then, in a first process step, a vitreous layer 50, preferably a BPSG layer, is applied on the polysilicon layer 40 and levelled preferably with the aid of a chemical mechanical blind polishing operation. A cross

30   section through the silicon wafer 1 after this process step is shown in Figure 2B.

Afterward, a resist layer 60 is applied and exposed by means of a perforated mask which defines the contact

35   openings for the bit line contacts between the mutually

adjacent gate electrode tracks 2. The resist layer 60 is
then developed, the exposed regions of the resist layer
being removed and the BPSG layer surface 50 being
uncovered in the region of the contact openings. A cross
5   section through the silicon wafer 1 after this process
step is illustrated in Figure 2C.

The patterned resist mask 60 is then used as an etching
mask for an anisotropic etching of the BPSG layer 50, the
10   structure of the contact openings in the resist layer 60
being transferred to the BPSG layer 50. A cross section
through the silicon wafer 1 after this anisotropic
etching of the BPSG layer 50 for the purpose of
uncovering the underlying polysilicon surface 40 in the
15   region of the envisaged contact openings is shown in
Figure 2D.

A contact hole filling with a second mask material, e.g.
an organic ARC material, is subsequently performed. A
20   large-area filling material deposition is preferably
carried out in this case. A cross section through the
silicon wafer after the large-area deposition of the ARC
layer 51 is illustrated in Figure 2E.

25   The ARC layer 51 is then removed again from the surface
of the BPSG layer 50, the etching-back being performed in
such a way that an overetching takes place and the ARC
layer 51 is also removed from an upper region of the
contact openings. A cross section through the silicon
30   wafer 1 after this ARC material etching-back is shown in
Figure 2F.

Finally, the BPSG layer 50 is then completely removed in
a further etching step, thereby producing an ARC material
35   block 51 in the region of the envisaged contact openings

for the bit line contacts between the mutual adjacent
gate electrode tracks 2, as is shown in cross section in
Figure 2G.

5   The structure of the ARC material plug may then be
transferred to the underlying polysilicon layer 4 by
means of a further etching, so that only the ARC material
plug with the underlying polysilicon region remains and a
structure as occurs in the case of the first embodiment,
10 in the process stage shown in Figure 1F, then results.
Afterward, if appropriate, the remaining ARC material may
then be removed again and the method continues with the
process sequence for forming the bit line contacts and
the first metallization plane, as is illustrated in
15 Figures 1G to 10.

The illustrated variant for forming the polysilicon plugs
which protect the contact openings makes it possible in
particular to dispense with additional complicated
20 polishing techniques for fabricating smooth surfaces on
the polysilicon layer, which are necessary for a resist
patterning with resist plugs. What is more, through the
use of the further hard mask layer made of a vitreous
material on the non plane base formed by the polysilicon
25 layer 40, the lithography process illustrated affords the
advantage that steps in said polysilicon layer 40 can be
utilized in a simple manner for mask orientation during
the contact hole lithography. The use of the BPSG layer
50 furthermore makes it possible to accurately set the
30 plug height above the contact openings and to use a
material such as ARC with high etching resistance for the
polysilicon etching in particular as a plug material,
thereby enabling the plug structure to be transferred
exactly to the polysilicon layer 40.

35

In the embodiments described previously, polysilicon has always been used as the material for the sacrificial layer for defining the contact hole openings. Polysilicon is distinguished by a particularly high selectivity when

5   etching free contact holes in particular with respect to the surrounded vitreous layer and also with respect to the surrounding gate electrode tracks. This is because it is possible to use, for the polysilicon etching, an isotropic etching preferably based on a halogen whilst

10   dispensing with virtually any sputtering element, i.e. without ion bombardment. This ensures that the polysilicon can be etched out completely, without damage in particular to the gate electrode tracks.

15   As an alternative to a sacrificial layer comprising polysilicon, however, it is also possible to use a different sacrificial layer material. In this case, a carbon-based layer is also suitable, in particular, as sacrificial layer material. Carbon can be removed in a

20   simple manner in the context of a conventional dry etching method using oxygen and is distinguished by a high selectivity with respect to other materials. Depending on the deposition process, the carbon-based layer can be applied in a simple manner and thus

25   cost-effectively with a high planarity, an additional planarization step generally not being necessary.

Figures 3A to 3D show a possible embodiment, again proceeding from a method stage as is shown in cross

30   section in Figure 1B, the gate electrode tracks 2, 20 having been applied on the prepatterned silicon wafer 1 in a first process step, the silicon dioxide layer 3 then having been deposited onto them in a large-area manner in a second process step. Proceeding from this process

35   stage, preferably a carbon layer 140 is then deposited in

a further process step. In this case, the layer thickness
of the carbon layer 140 preferably corresponds to at
least one to three times the height of the gate electrode
tracks 2, 20. Figure 3A shows a cross section through the
5   silicon wafer after this process step.

In the illustration shown in Figure 3A, the topology of
the underlying gate electrode tracks 2, 20 on the silicon
wafer 1 can be discerned on the surface of the carbon
10   layer 140. However, it is also possible to control the
deposition process of the carbon-containing layer in such
a way that an essentially plane carbon layer surface is
produced. In this case, the further process step shown in
Figure 3B, in which the surface of the carbon layer 140
15   is planarized, is then unnecessary.

Afterward, as shown in Figure 3C, a thin hard mask layer
141 made of silicon oxide, silicon nitride or silicon
oxide-nitride is additionally deposited on the planar
20   carbon layer surface. The regions of the bit line
contacts for the connection of the selection transistors
of the memory cells in the silicon wafer 1 are then
defined on the hard mask layer 141 once again with the
aid of lithography technology, as already illustrated
25   with reference to Figure 1F in the case of the process
sequence shown in Figure 1. For this purpose, a resist
layer 160 is patterned in such a way that the resist
plugs shown in Figure 3C remain above the contact
openings for the bit line contacts between the mutually
30   adjacent gate electrode tracks 2, 20.

In a next process step, the hard mask layer 141 is then
prepatterned and, in a further process step, the
prepatterning is transferred into the carbon layer by
35   means of an etching which is selective with respect to

the hard mask layer. In this case, it is possible to achieve higher etching rates than in the case of polysilicon. The result then is a cross section of the silicon wafer as is illustrated in Figure 3D, in which

5   carbon plugs conceal the contact openings between the gate electrode tracks highly precisely and accurately.

Afterward, the process sequence shown in Figures 1H to 1O may then be carried out, the etching free of the

10 remaining carbon layer plugs between the gate electrode tracks being effected by a simple dry etching using oxygen highly selectively with respect to the surrounded vitreous layer. As an alternative to the process sequence shown in Figures 3A to 3D, it is also possible to form

15 the carbon layer plugs in accordance with the process sequences shown in Figures 1 and 2, respectively.